WHAT IS CLAIMED IS:

1. A liquid crystal display, comprising:

a first insulating substrate;

a plurality of gate lines formed at the first substrate to transmit scanning signals;

a plurality data lines crossing over the gate lines to transmit picture signals;

a second insulating substrate facing the first substrate;

a liquid crystal layer injected into the gap between said first insulating substrate and said second insulating substrate;

a pixel demarcated by the gate lines and the data lines, the gate lines demarcating the pixels into rows, and the data lines demarcating the pixels into columns;

a black matrix defining each pixel;

a pixel electrode formed at each pixel; and

a storage capacitor formed between said pixel electrode and the previous gate line;

wherein an opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows.

2. The liquid crystal display of claim 1, wherein the opening ratio of the first pixel row is lower than the opening ratio of the other pixel rows.

3. The liquid crystal display of claim 2, wherein the difference in the opening ratio is made by differentiating an opening area of the black matrix.

4. The liquid crystal display of claim 3, wherein the black matrix is formed at the second substrate.

5. The liquid crystal display of claim 2, wherein the difference in the opening ratio is made by forming a light interception pattern at each pixel of the first pixel row.

6. The liquid crystal display of claim 5, wherein the light interception pattern is formed at the same layer as the data line with the same material.

7. The liquid crystal display of claim 5, wherein the light interception pattern is formed at the same layer as the gate line with the same material.

8. The liquid crystal display of claim 2, wherein the opening ratio of the first pixel row is designed to be 60-80% of the opening ratio of the other pixel rows.

9. A liquid crystal display, comprising:

a first insulating substrate;

a plurality of gate lines formed at the first substrate to transmit scanning signals;

a plurality of data lines crossing over the gate lines to transmit picture signals;

a second insulating substrate facing the first substrate;

a liquid crystal layer injected into the gap between said first insulating substrate and said second insulating substrate;

a pixel demarcated by the gate lines and the data lines, the gate lines demarcating the pixels into rows, and the data lines demarcating the pixels into columns;

a black matrix defining each pixel;

a pixel electrode formed at each pixel;

a storage capacitor line formed on said first insulating substrate parallel to the gate line, the storage capacitor line overlapping the pixel electrodes at the first pixel row;

a first storage capacitor formed between said pixel electrode and the previous gate line; and,

a second storage capacitor formed between said pixel electrode and said storage capacitor line;

wherein a gate-off voltage or a common electrode voltage is applied to said storage capacitor line.

10. The liquid crystal display of claim 9, wherein an opening ratio of each pixel at the first pixel row is different from the opening ratio of the pixels at the other pixel rows.

11. The liquid crystal display of claim 10, wherein the opening ratio of the first pixel row is lower than the opening ratio of the other pixel rows.

12. The liquid crystal display of claim 11, wherein the difference in the opening ratio is made by differentiating an opening area of said black matrix.

13. The liquid crystal display of claim 12, wherein said black matrix

is formed at said second substrate.

14. The liquid crystal display of claim 13, wherein opening width of said black matrix at the first pixel row in the longitudinal direction of the gate line is identical to opening width of said black matrix at the other pixel rows.

15. The liquid crystal display of claim 13, wherein opening length of said black matrix at the first pixel row in the longitudinal direction of the gate line is shorter than opening length of said black matrix at the other pixel rows.

16. The liquid crystal display of claim 11, wherein a difference in the opening ratio is made by forming a light interception pattern at each pixel of the first pixel row.

17. The liquid crystal display of claim 16, wherein the light interception pattern is formed at the same layer as the data line with the same material.

18. The liquid crystal display of claim 17, wherein the light interception pattern is formed at the same layer as the gate line with the same material.

19. The liquid crystal display of claim 11, wherein the opening ratio of the first pixel row is designed to be 60-80% of the opening ratio of the other pixel rows.

20. The liquid crystal display of claim 9, further comprising a gate-off line formed on said first substrate to transmit a gate-off voltage.

21. The liquid crystal display of claim 20, wherein the gate-off line and said storage capacitor line are formed at the same layer as the gate line.

22. The liquid crystal display of claim 21, wherein the gate-off line and said storage capacitor line are electrically connected to each other via a connection member, and the connection member is formed at the same layer as the data line or said pixel electrode.

23. The liquid crystal display of claim 9, further comprising gate signal transmission films arranged at said first substrate and provided with a gate driving integrated circuit that is electrically connected to the gate lines and outputs gate driving signals, and data signal transmission films arranged at said first substrate and provided with a data driving integrated circuit that is electrically connected to the data lines and outputs data driving signals,

wherein a common electrode wire for applying the common electrode voltage (Vcom), a gate-on wire for applying the on-voltage Von to the TFTs controlling the picture signals, a gate-off wire for applying the off-voltage Voff, and wires for transmitting carry-in or gate-clock signals are formed on the edge portion of the first substrate between the gate signal transmission film and the data signal transmission film.

24. The liquid crystal display of claim 23, the common electrode wire, the gate-on wire and the gate-off wire are formed at the same layer as the gate lines with the same material.

25. A liquid crystal display, comprising:

a first insulating substrate;

a plurality of first signal lines formed on said first substrate;

a first pad connected to an end portion of the first signal line, said first

pad being connected to external driving circuits;

a plurality of second signal lines crossing over the first signal lines to form a pixel area, the pixel area collectively forming a display area;

a second pad connected to an end portion of the second signal line, said second pad being connected to external driving circuits; and

a first light interception pattern positioned outside of the display area, said first light interception pattern being electrically insulated from the first signal lines and said first pads.

26. The liquid crystal display of claim 25, wherein the first light interception pattern does not overlap the first signal lines and said first pad.

27. The liquid crystal display of claim 26, wherein the first light interception pattern lies between the display area and said first pad.

28. The liquid crystal display of claim 27, wherein the first light interception pattern is spaced apart from said first pad by a predetermined distance.

29. The liquid crystal display of claim 25, wherein the first light interception pattern is formed at the same layer as the second signal lines.

30. The liquid crystal display of claim 25, further comprising a second light interception pattern positioned outside of the display area, the second light interception pattern being electrically insulated from the second signal lines and a second pad.

31. The liquid crystal display of claim 30, wherein the second light interception patterns are formed at the same layer as the first signal lines.

32. The liquid crystal display of claim 25, further comprising a second insulating substrate facing the first insulating substrate.

33. The liquid crystal display of claim 32, further comprising a black matrix defining each pixel area.

34. The liquid crystal display of claim 33, wherein the first light interception pattern and the second light interception pattern overlap the black matrix.

35. The liquid crystal display of claim 32, further comprising a sealer that seals the first insulating substrate with the second insulating substrate surrounding the display area.

36. The liquid crystal display of claim 35, wherein the first light interception pattern and the second light interception pattern do not overlap the sealer.

37. The liquid crystal display of claim 32, further comprising a color filter formed on the pixel areas.

38. The liquid crystal display of claim 32, further comprising a common electrode formed on the second insulating substrate.

39. The liquid crystal display of claim 25, further comprising a thin film transistor connected to the first signal line and the second signal line, and a pixel electrode positioned at the pixel areas.

40. A liquid crystal display, comprising:

a first insulating substrate;

a gate line assembly formed at said first insulating substrate, said gate

line assembly comprising a plurality of gate lines, gate electrodes branched from the gate lines, and gate pads connected to the gate lines to transmit scanning signals thereto;

a first light interception pattern isolated from said gate line assembly;

a gate insulating layer covering said gate line assembly and said first light interception pattern;

a semiconductor layer formed on said gate insulating layer;

a data line assembly formed on said semiconductor layer and said gate insulating layer, said data line assembly comprising a plurality of data lines crossing over the gate lines while forming pixel areas, source electrodes branched from the data lines, drain electrodes positioned opposite to the source electrodes while centering around the gate electrodes, and data pads connected to the data lines to transmit picture signals thereto, the pixel areas collectively forming a display area;

a second light interception pattern isolated from said data line assembly;

a protective layer covering said data line assembly and said second light interception pattern, the protective layer having first to third contact holes exposing the gate pad, the data pad and the drain electrode, respectively; and

a pixel electrode connected to the drain electrode via the third contact hole;

wherein said first light interception pattern and said second light interception pattern are positioned outside of the display area.

41. The liquid crystal display of claim 40, wherein said first light interception pattern and said second light interception pattern do not overlap the gate lines and the data lines.

42. The liquid crystal display of claim 40, wherein said first light interception pattern and said second light interception pattern are spaced apart respectively from the gate pads and the data pads by a predetermined distance.

43. The liquid crystal display of claim 40, further comprising:

a second insulating substrate facing the first substrate;

a color filter formed at said second substrate corresponding to the pixel areas;

a black matrix formed at the second substrate surrounding said color filter; and

a common electrode covering said color filter and said black matrix.

44. The liquid crystal display of claim 43, wherein said first light interception pattern and said second light interception pattern overlap the black matrix.

45. The liquid crystal display of claim 43, further comprising a sealer sealing said first insulating substrate and said second insulating substrate.

46. The liquid crystal display of claim 45, wherein said first light interception pattern and said second light interception pattern do not overlap the sealer.

47. The liquid crystal display of claim 40, further comprising an ohmic contact layer formed on the semiconductor layer.

48. The liquid crystal display of claim 40, further comprising a subsidiary gate pad covering each gate pad via the first contact hole, and a subsidiary data pads covering each data pad via the second contact hole.

49. A method for fabricating a liquid crystal display, comprising the steps of:

forming a gate line assembly and a first light interception pattern on a first insulating substrate such that the first light interception pattern is separated from the gate line assembly;

forming a gate insulating layer such that the gate insulating layer covers the gate line assembly and the first light interception pattern;

forming a semiconductor layer on the gate insulating layer;

forming an ohmic contact layer on the semiconductor layer;

forming a data line assembly and a second light interception pattern such that the data line assembly crosses over the gate line assembly while forming pixel areas and the second light interception patterns are separated from the data line assembly, the pixel areas collectively forming a display area, the first light interception pattern and the second light interception pattern being positioned outside of the display area;

forming a protective layer such that the protective layer covers the data line assembly and the second light interception pattern; and

forming a pixel electrode on the protective layer.

50. The method of claim 49, wherein the first light interception pattern and the second light interception pattern do not overlap the data line assembly and the gate line assembly.

51. The method of claim 49, wherein the semiconductor layer, the ohmic contact layer, the data line assembly, and the second light interception patterns are formed together in one photolithography process.

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